ABSTRACT OF THE DISCLOSURE

[0025] A processor may include a local addressable memory, e.g., an SRAM, in parallel with a local cache at the highest level of the memory hierarchy, e.g., Level 1 (L1) memory. A local memory controller may handle accesses to L1 memory. The local memory controller may determine the page which includes the requested memory location and examine a page descriptor, e.g., an L1 SRAM bit, to determine if the page is in local memory. The local memory controller routes the access to the local addressable memory or the local cache depending on the state of the L1 SRAM bit.